METHOD OF REDUCING LEAKAGE CURRENT IN SUB ONE VOLT SOI CIRCUITS

ABSTRACT OF THE INVENTION

A multi-threshold integrated circuit (IC) with reduced subthreshold leakage and method of reducing leakage. Selectable supply switching devices (NFETs and/or PFETs) between a logic circuit and supply connections (V_{dd} and Ground) for the circuit have higher thresholds than normal circuit devices. Some devices may have thresholds lowered when the supply switching devices are on. Header/footer devices with further higher threshold voltages and widths may be used to further increase off resistance and maintain/reduce on resistance. Alternatively, high threshold devices may be stacked to further reduce leakage to a point achieved for an even higher threshold. Intermediate supply connects at the devices may have decoupling capacitance and devices may be tapered for optimum stack height and an optimum taper ratio to minimize circuit leakage and circuit delay.